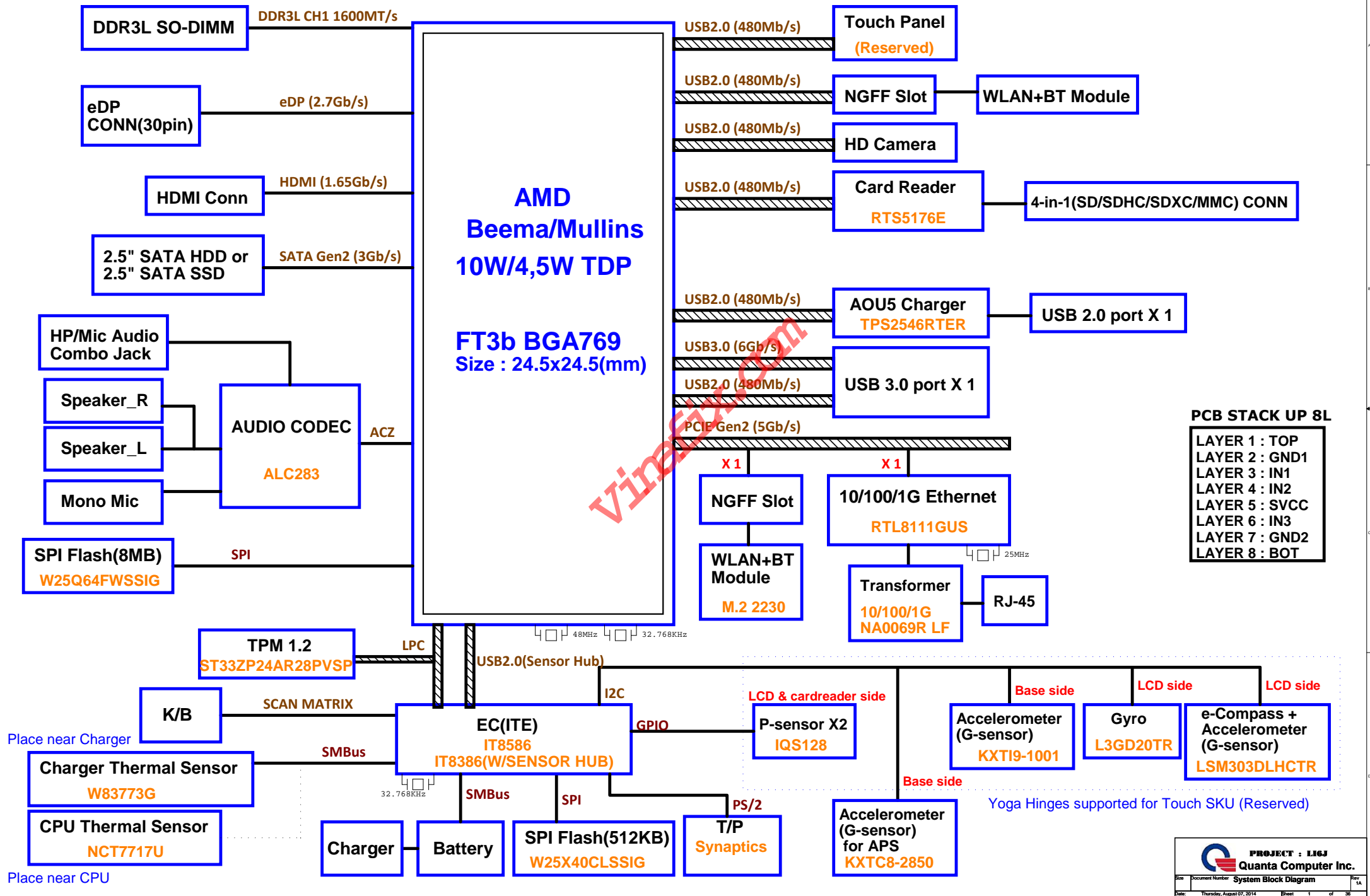



MR1.5 AMD Beema Platform UMA Block Diagram (Windows)

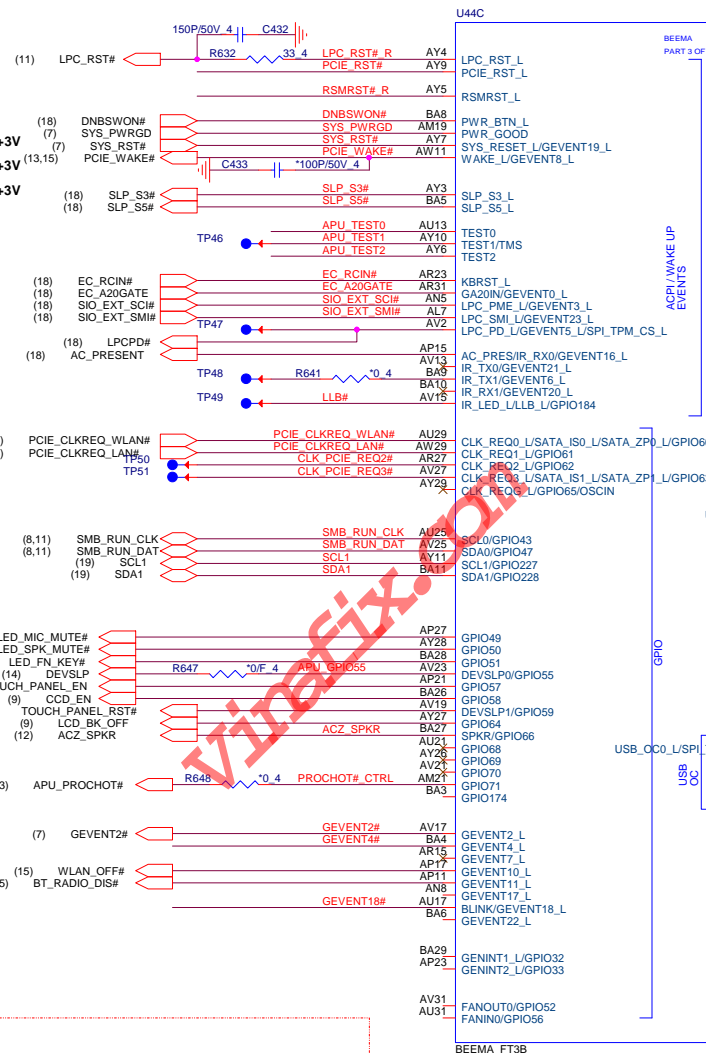




Place within 1000mil of the APU



1.35V_SUS
+VREF_DQ
0.95V



3.3V

R644 2.2K SMB_RUN_CLK

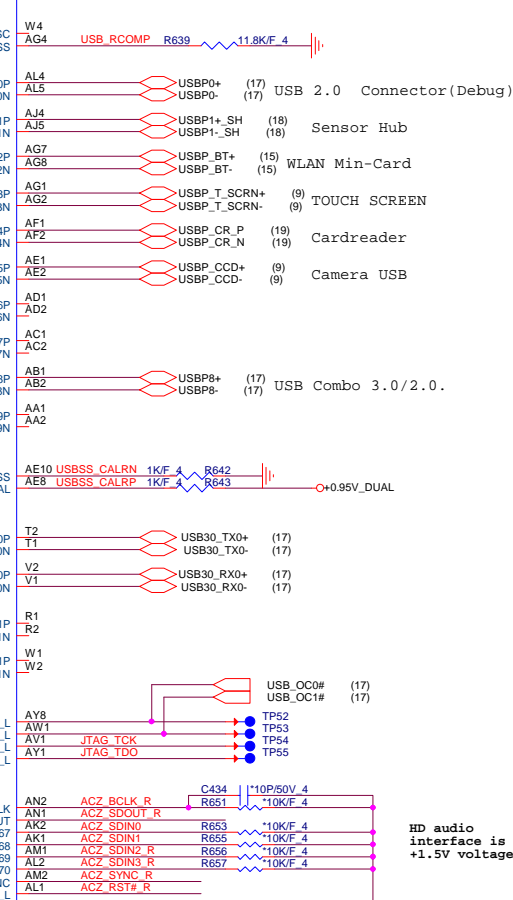
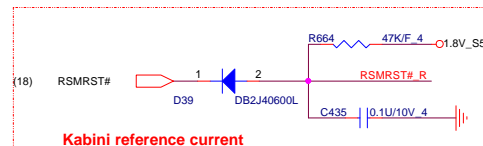
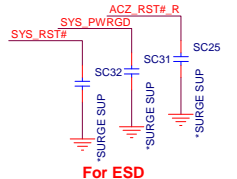
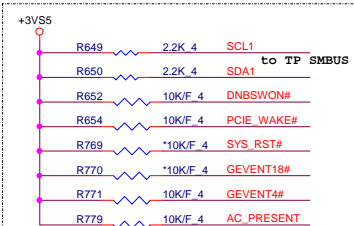
R645 2.2K SMB_RUN_DAT to DDR3 SMBUS

3VSS R646 1K/F 4

J2 1 2 SYS_RST#

*SOLDERJUMPER-2

SYS_RST# internal 10K pull up

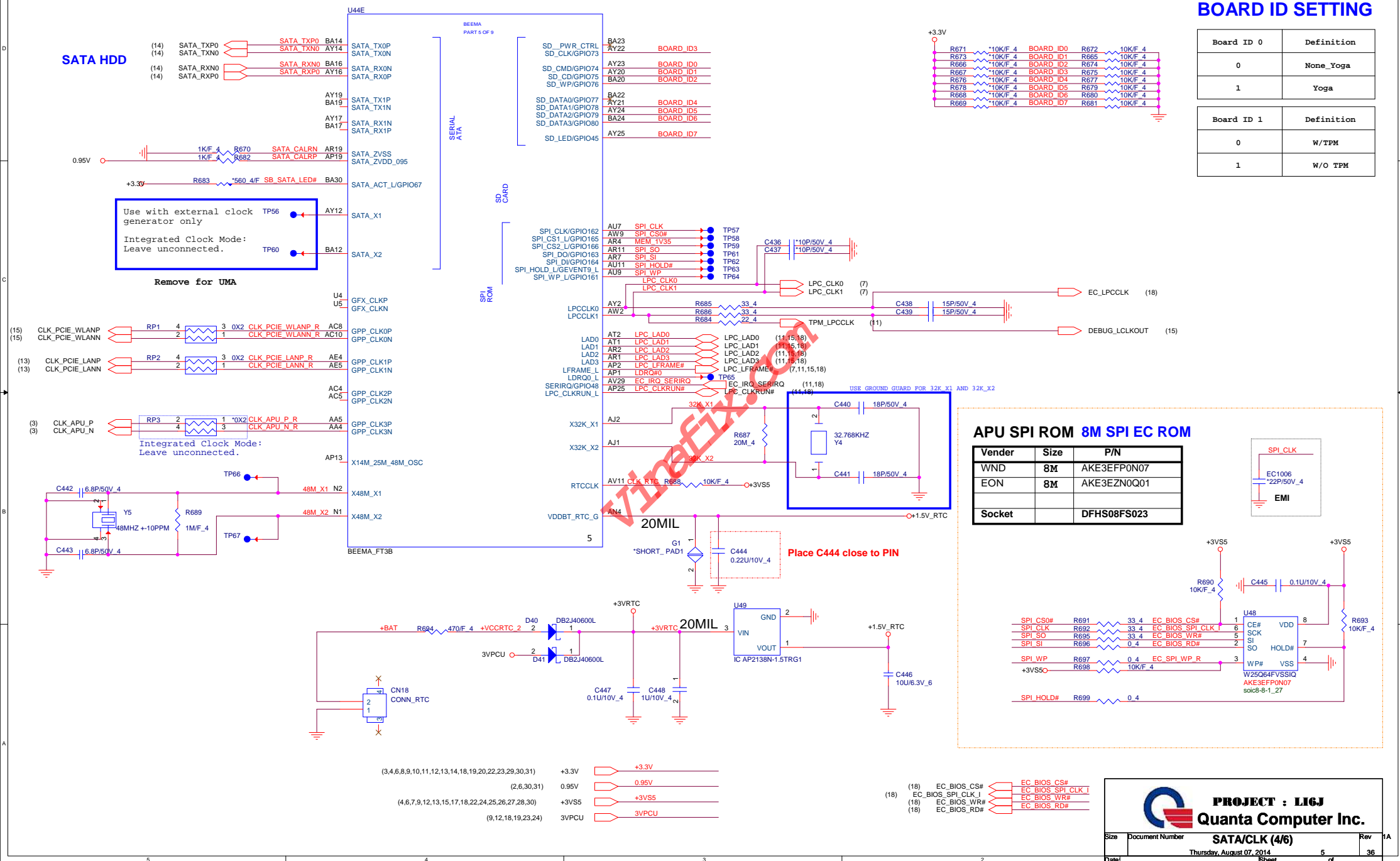


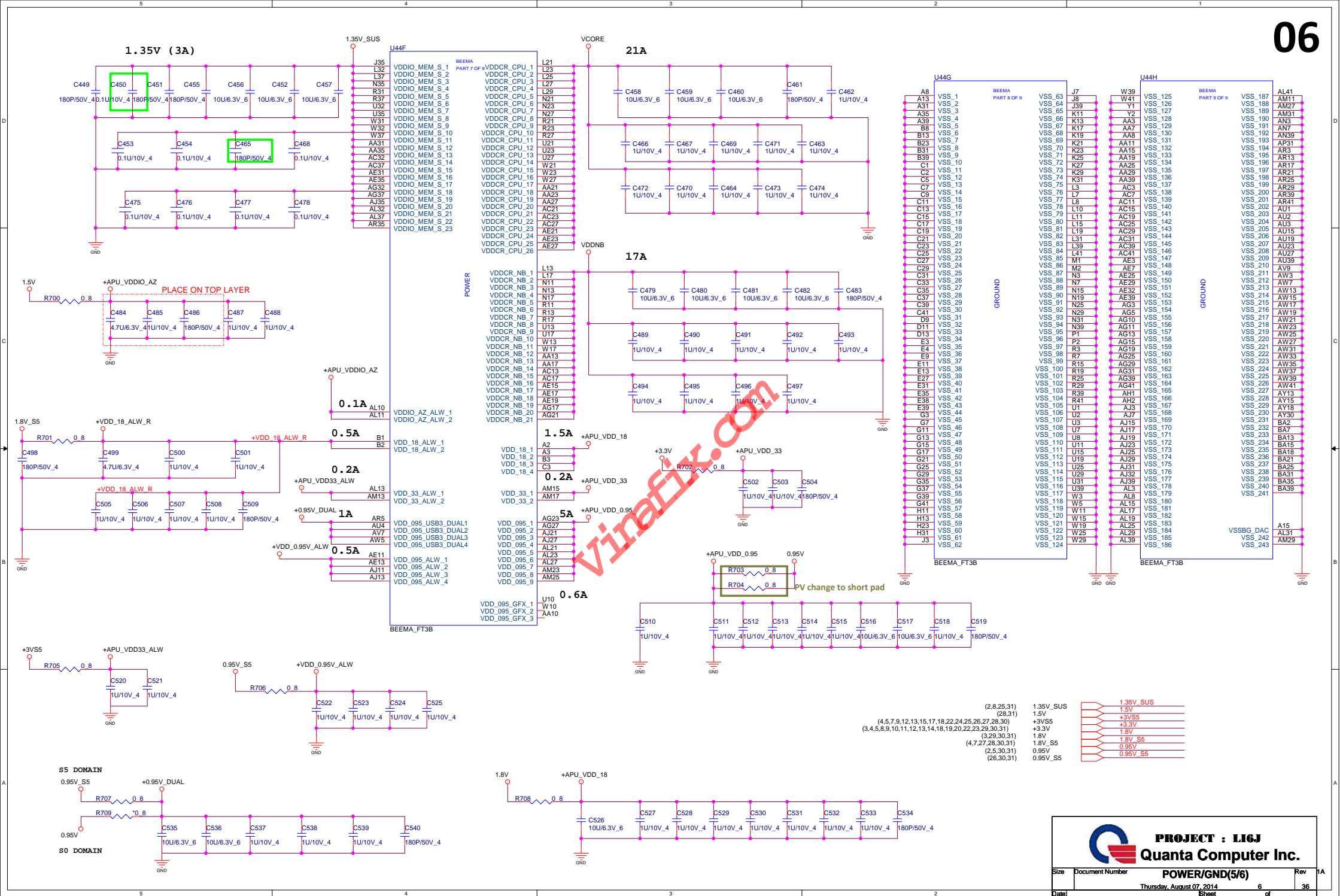
ACZ_SDOUT_R	R660	33_4	ACZ_SDOUT_AUDIO	(12)
ACZ_SYNC_R	R661	33_4	ACZ_SYNC_AUDIO	(12)
ACZ_BCLK_R	R662	33_4	BIT_CLK_AUDIO	(12)
ACZ_RST#_R	R663	33_4	ACZ_RST#_AUDIO	(12)
ACZ_SDINO			ACZ_SDINO	(13)

BOARD ID SETTING

Board ID 0	Definition
0	None_Yoga
1	Yoga

Board ID 1	Definition
0	W/TPM
1	W/O TPM

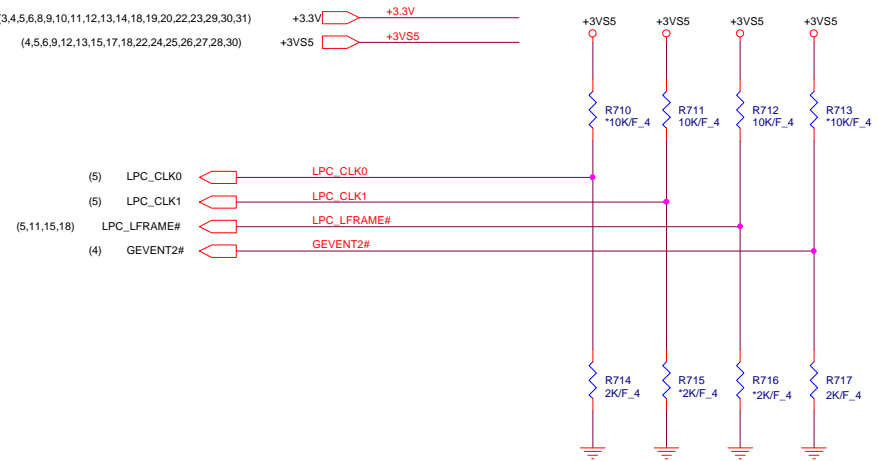






STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

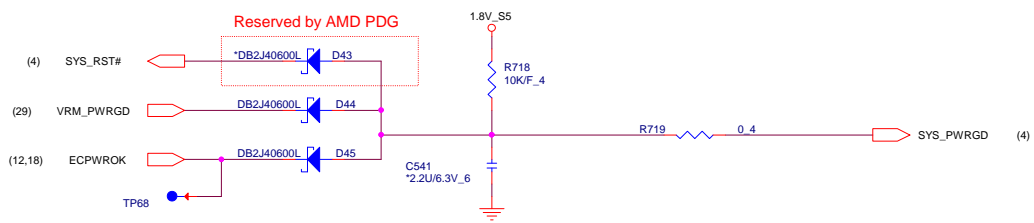


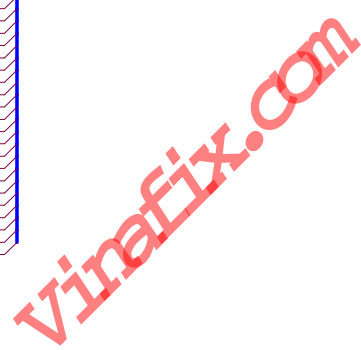
REQUIRED STRAPS

PULL HIGH					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW					BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

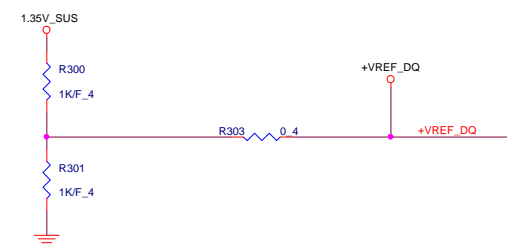
DEBUG STRAPS

SYS_PWRGD





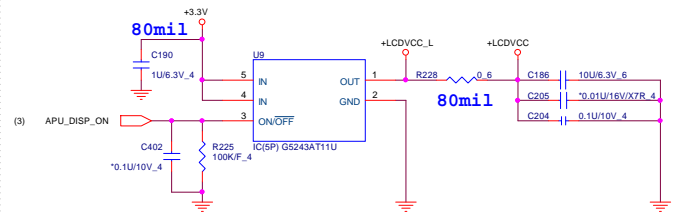
Reserved for AMD suggest



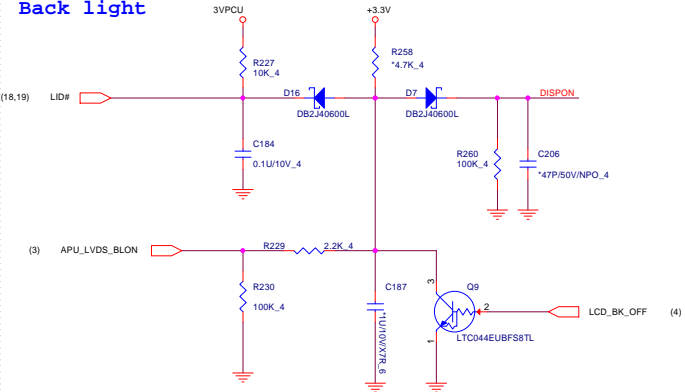
PROJECT : LI6J
Quanta Computer Inc.

Size	Document Number	System Memory 2/2 (4.0H)		Rev
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Date:		Sheet	8 of	36

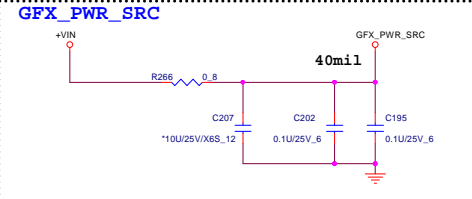
LCDVCC



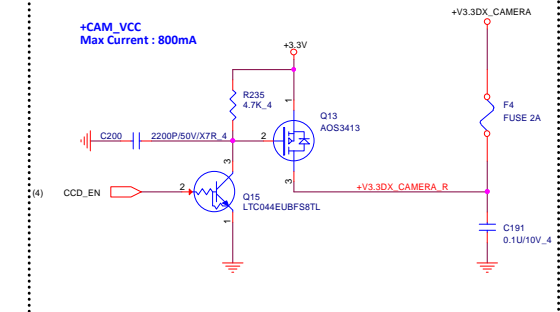
Back light



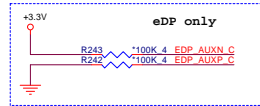
GFX_PWR_SRC



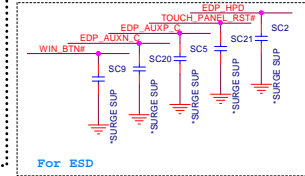
CAMERA VCC Control



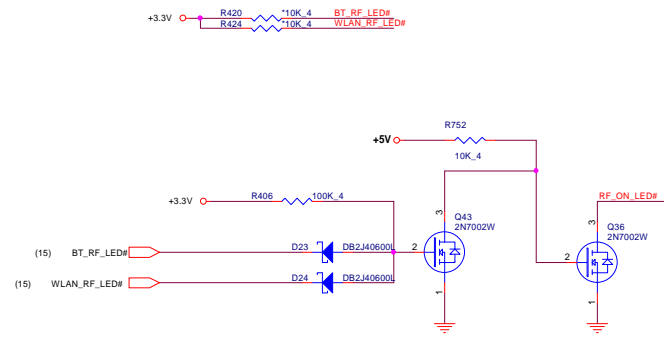
eDP only



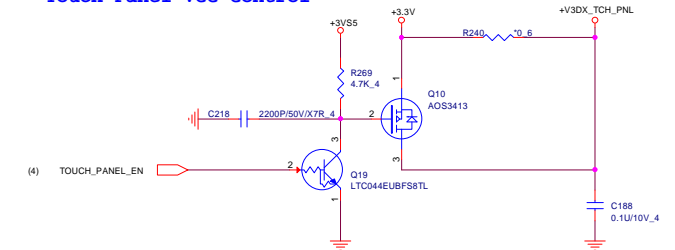
Touch Panel



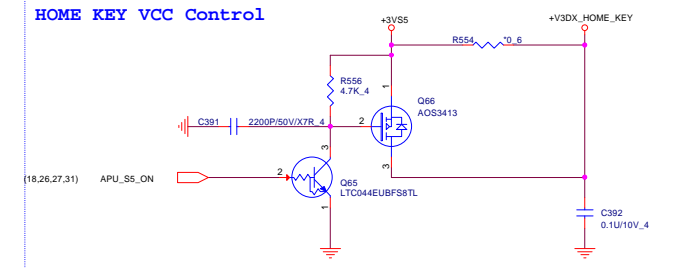
CCD+MIC+LOGO+WLAN LED CONN



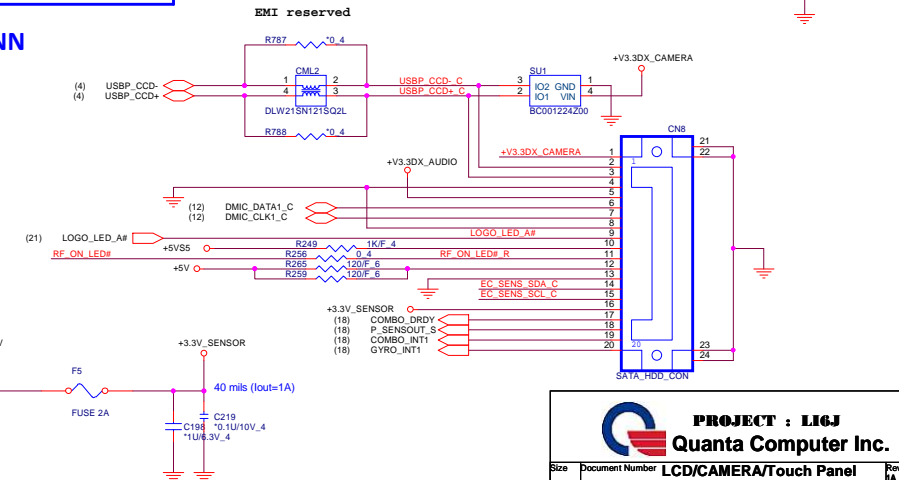
Touch Panel VCC Control

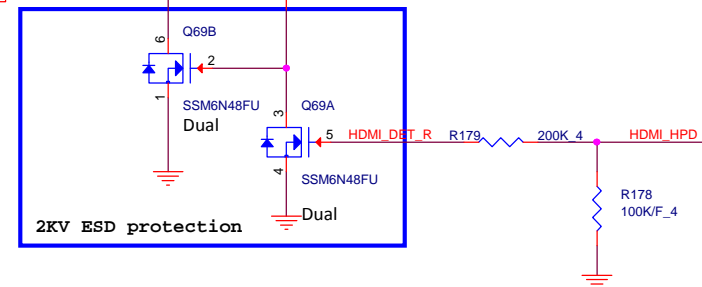
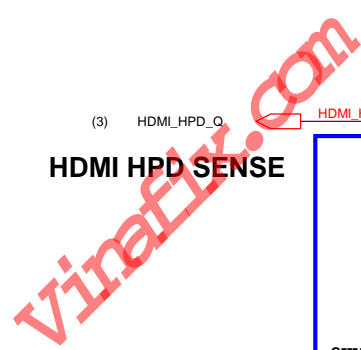


HOME KEY VCC Control



EMI reserved





HDMI_TX2+_C

R254
*150/F_4

HDMI_TX2-_C

HDMI_TX1+_C

R263
*150/F_4

HDMI_TX1-_C

HDMI_TX0+_C

R268
*150/F_4

HDMI_TX0-_C

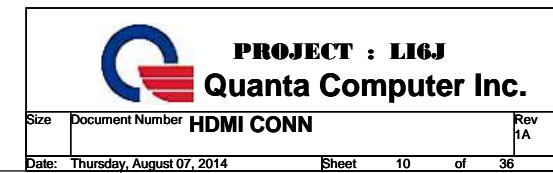
HDMI_CLK+_C

R280
*150/F_4

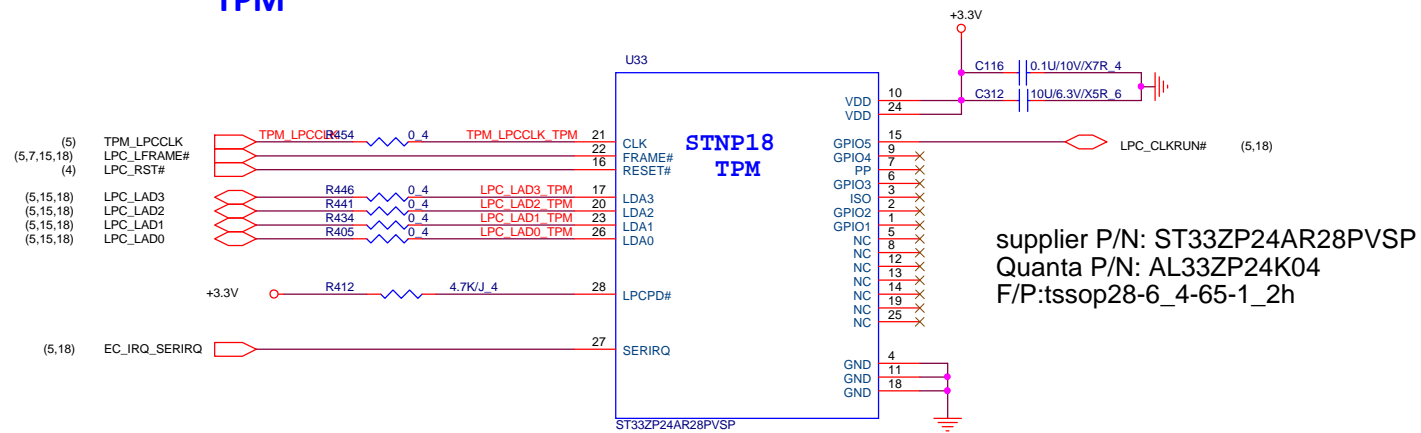
HDMI_CLK-_C

HDMIC_5V

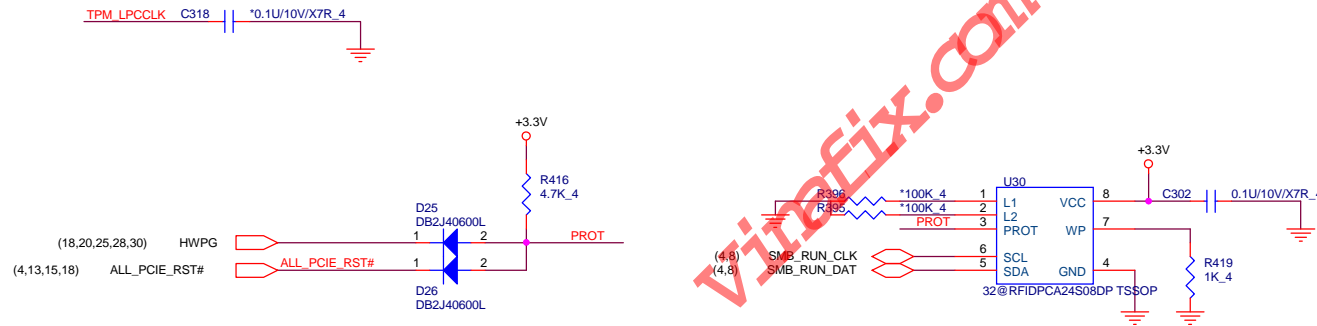
EC5
UCLAMP0511P.TCT



TPM



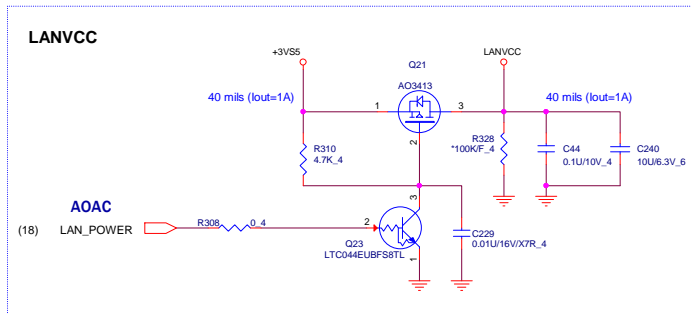
RFID



PROJECT : LIGJ
Quanta Computer Inc.

Size	Document Number	Rev
	TPM/RFID	1A

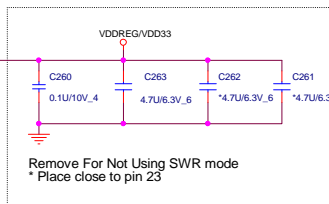
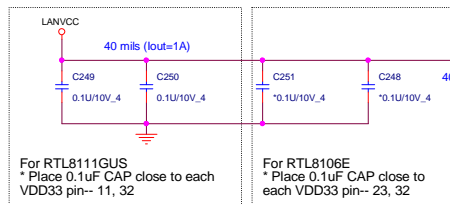
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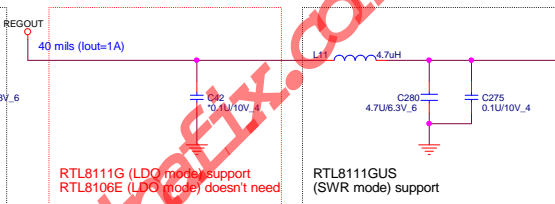
LANVCC
Trace width>60mil,
Trace length<200mil

B-stage only 10/100 config.

10/100	RTL8106EUS-CG	AL008106002
1G	RTL8111GUS-CG	AL008111009

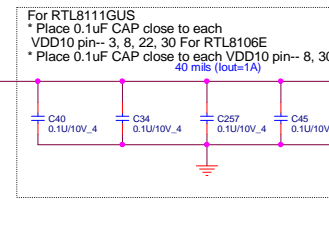


Remove For Not Using SWR mode
* Place close to pin 23



RTL8111G (LDO mode) support
RTL8106E (LDO mode) doesn't need

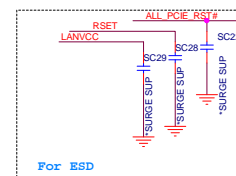
RTL8111GUS
(SWR mode) support



For RTL8111GUS
* Place 0.1uF CAP close to each
VDD10 pin-- 3, 8, 22, 30 For RTL8106E
* Place 0.1uF CAP close to each VDD10 pin-- 8, 30

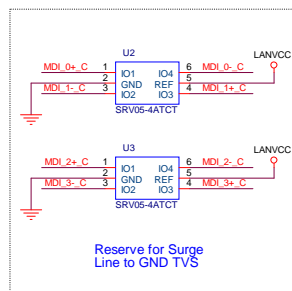
For RTL8106E
* Place 1uF CAP close to each VDD10 pin-- 30 (reserve)

For RTL8111GUS
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

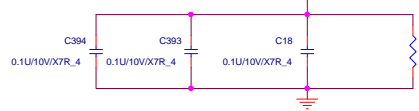


For ESD

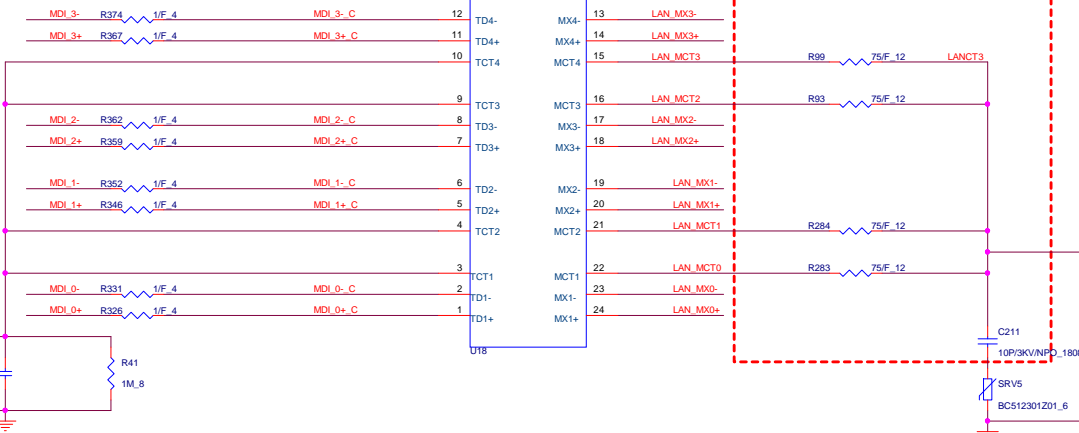
Transformer



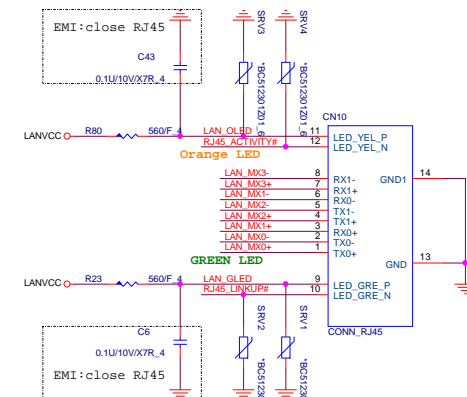
Reserve for Surge
Line to GND TVS

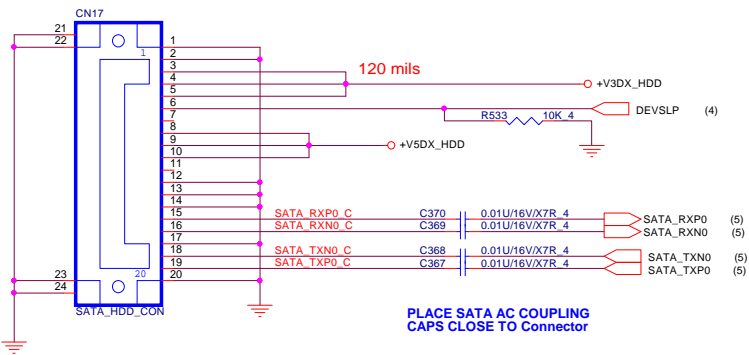


Layout: All termination
signal should have 50 mil
trace / 50mil spacing

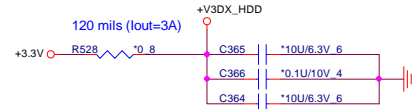


RJ45 Connector

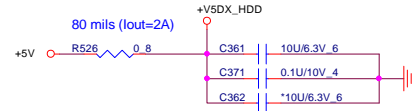




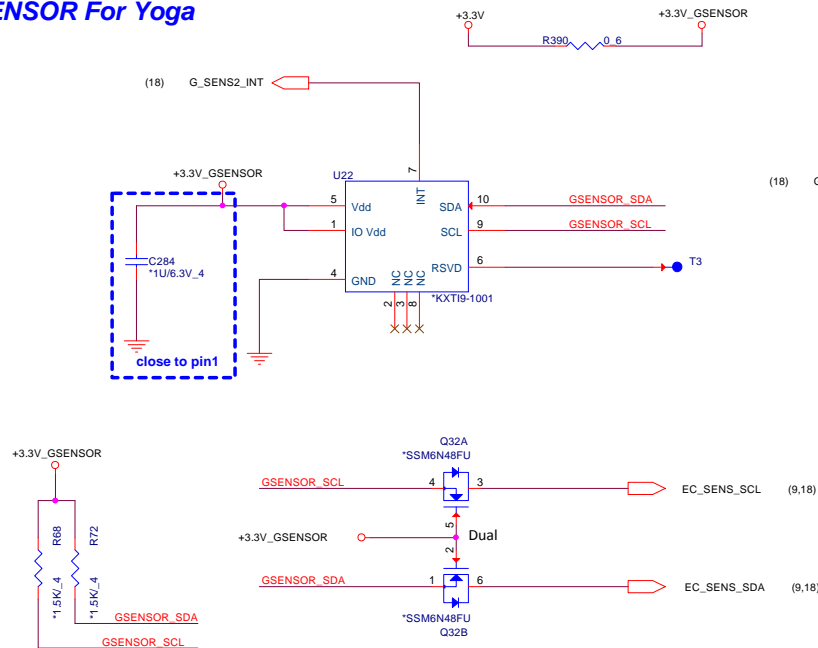
DC Current rating: 3 A (MAX)



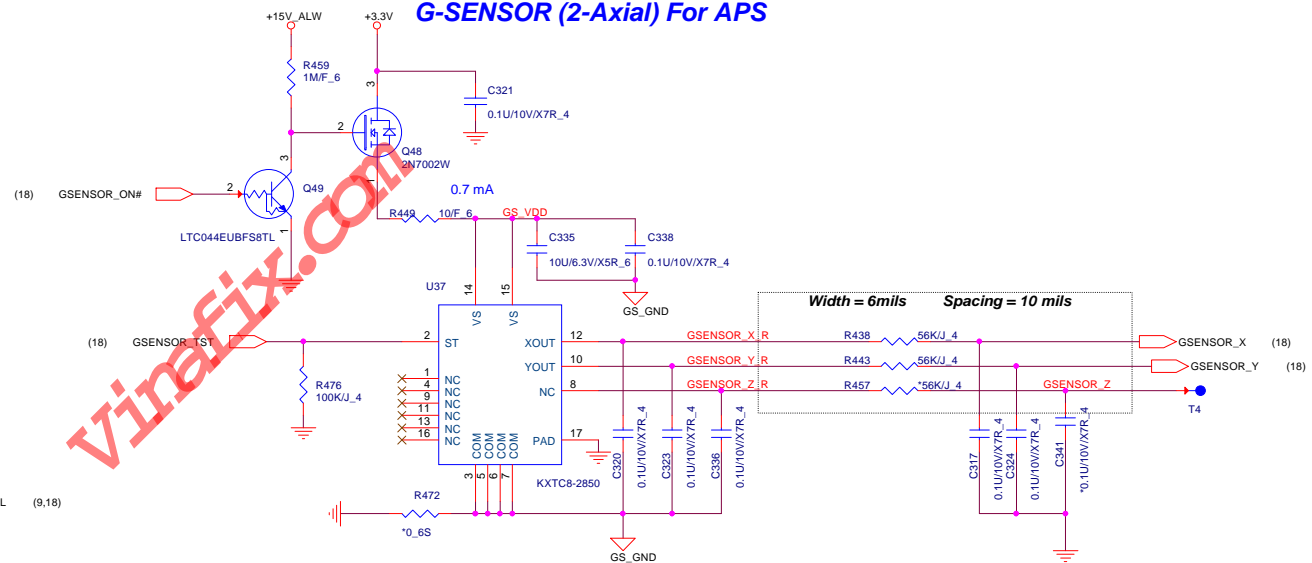
DC Current rating: 2 A (MAX)



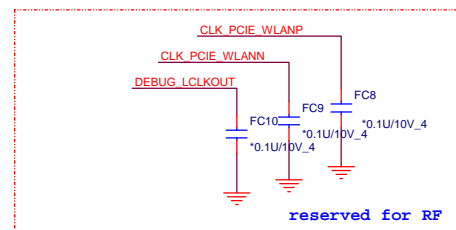
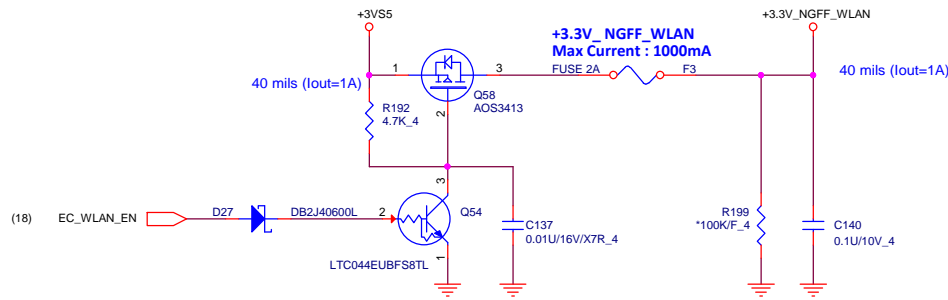
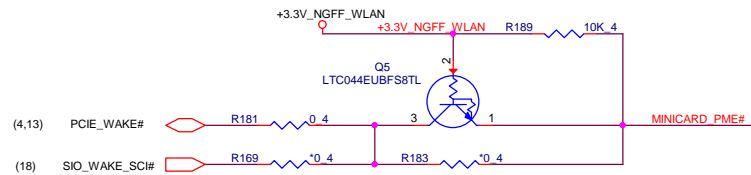
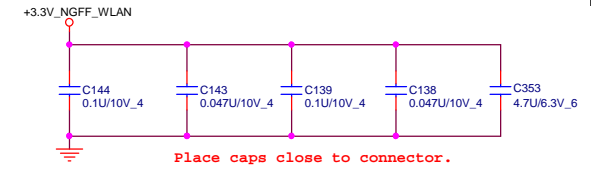
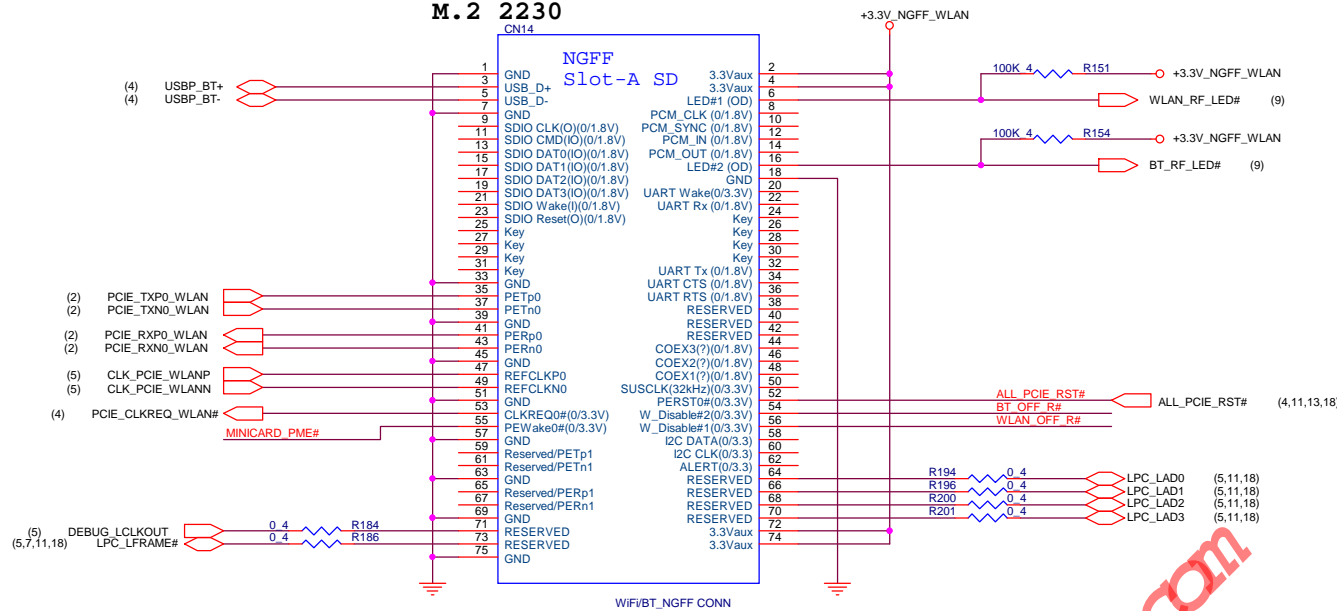
G-SENSOR For Yoga



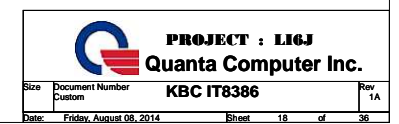
G-SENSOR (2-Axial) For APS



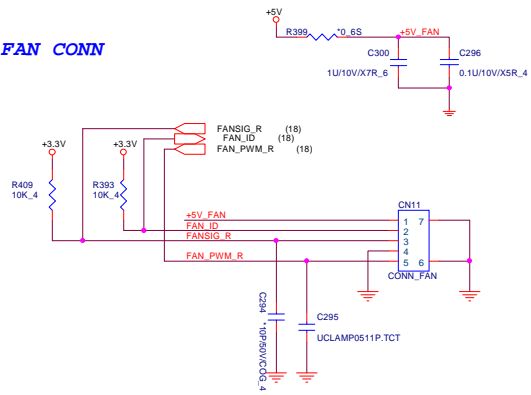
NGFF WiFi/BT connector M.2 2230



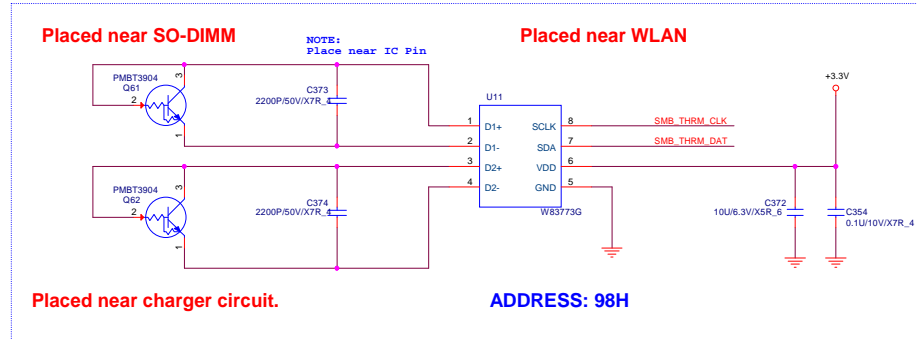
[illegible]



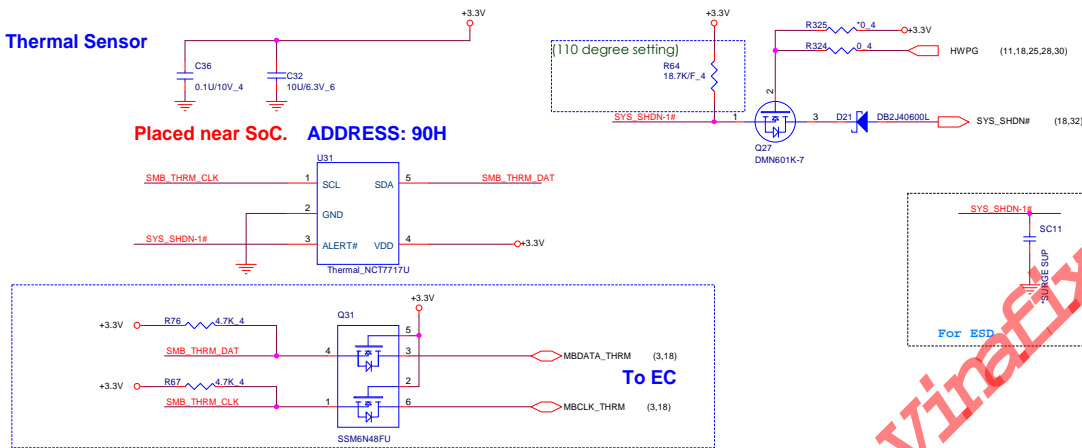
FAN CONN

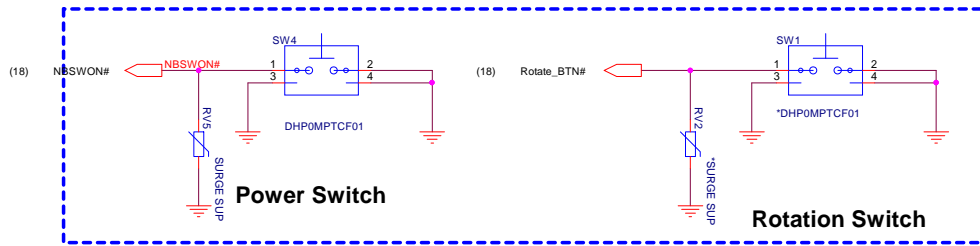


Thermal Sensor

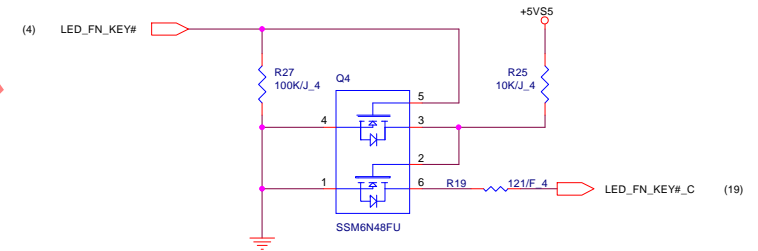
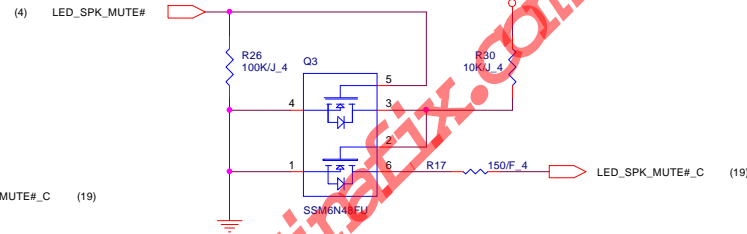
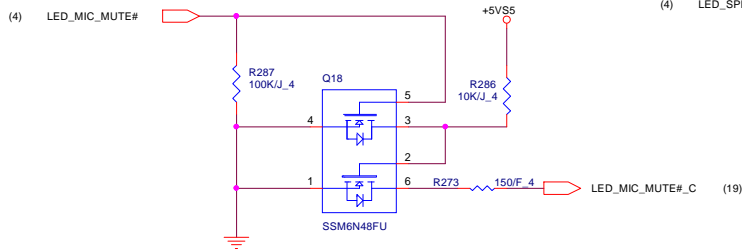
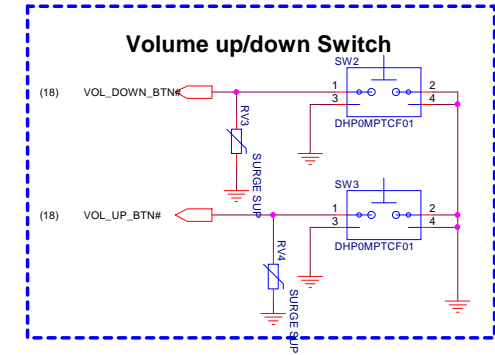
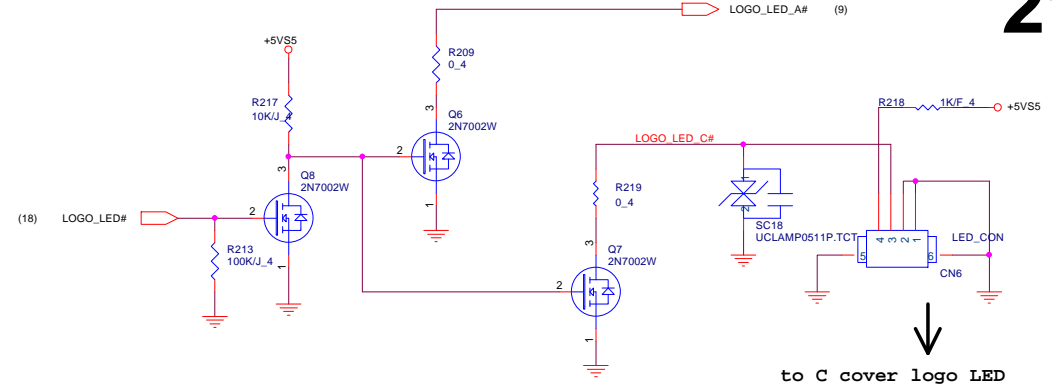


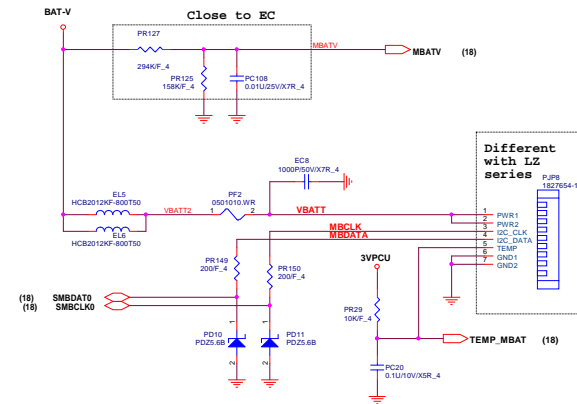
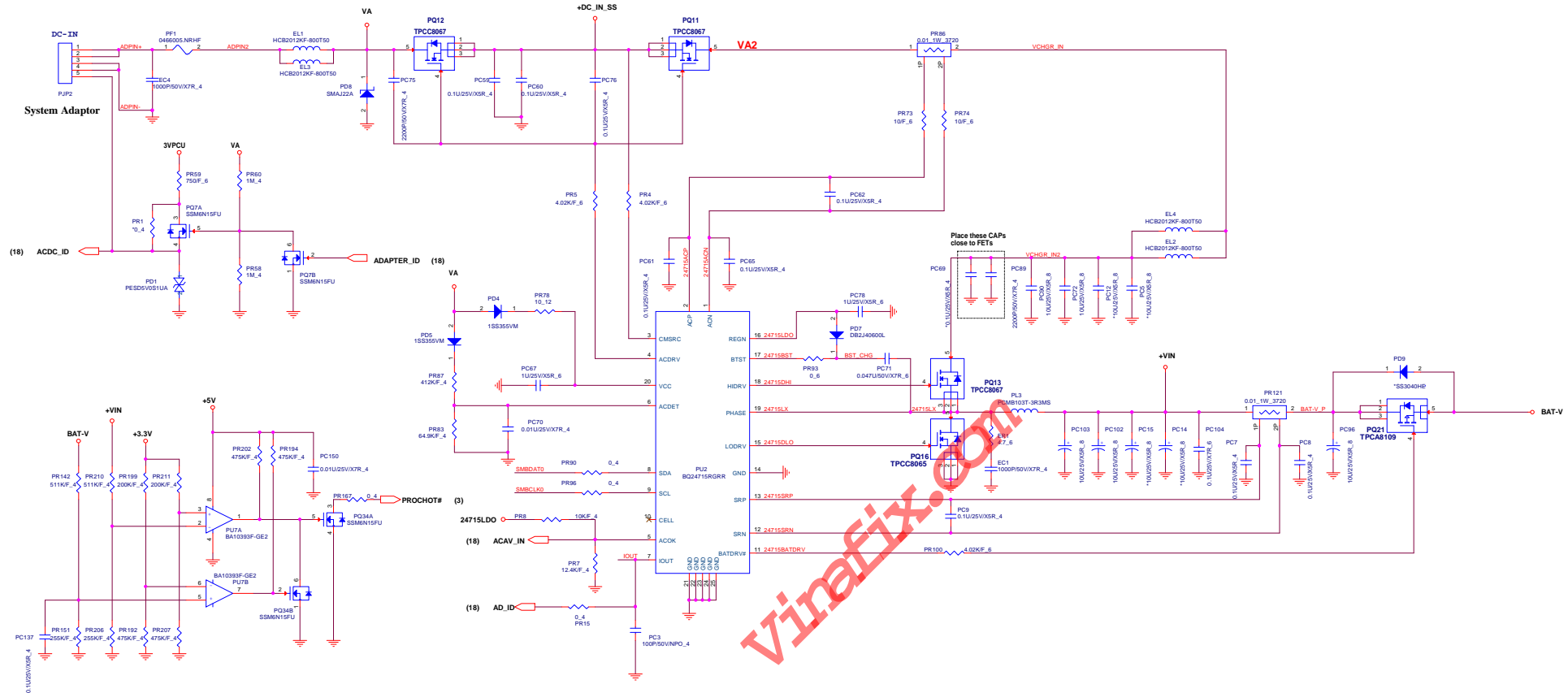
CPU Thermal Sensor





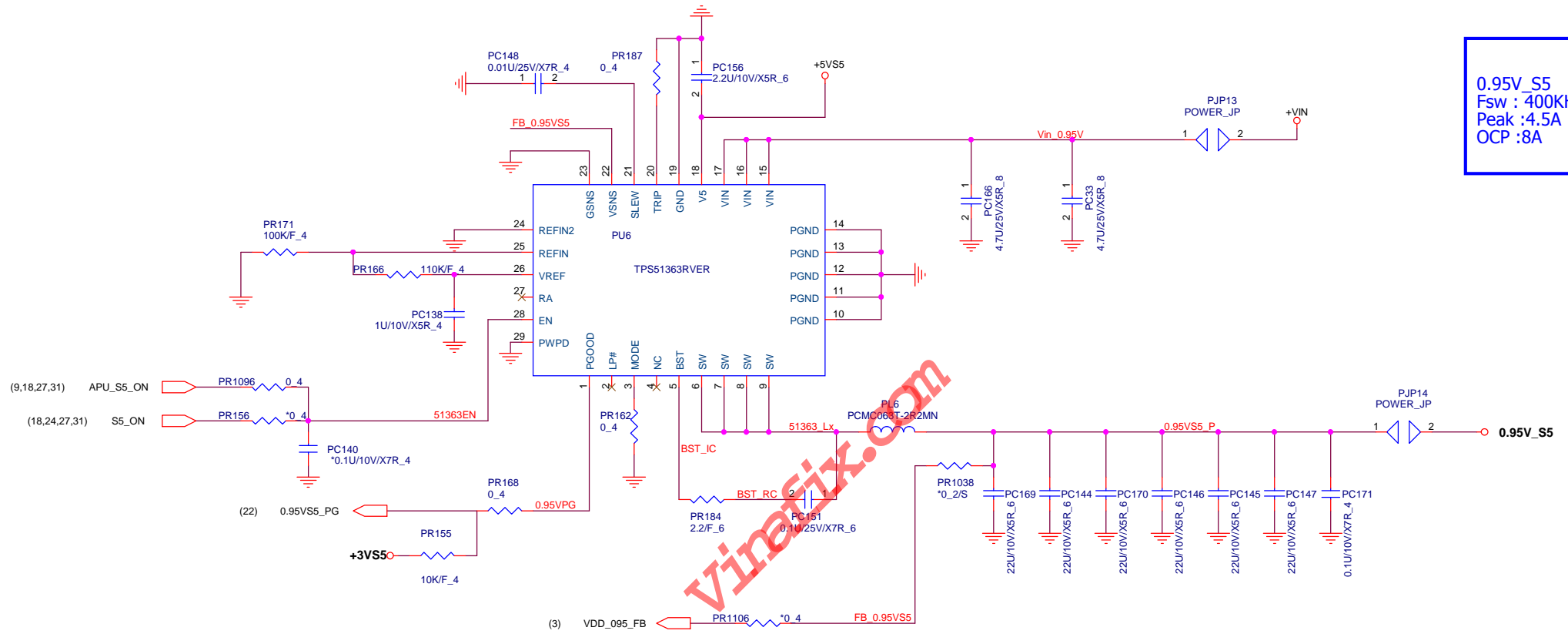
LED Driver





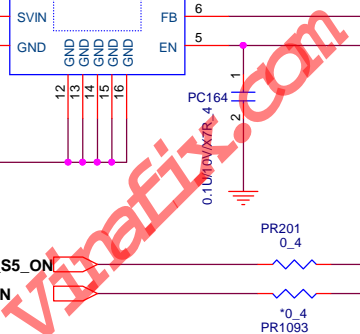




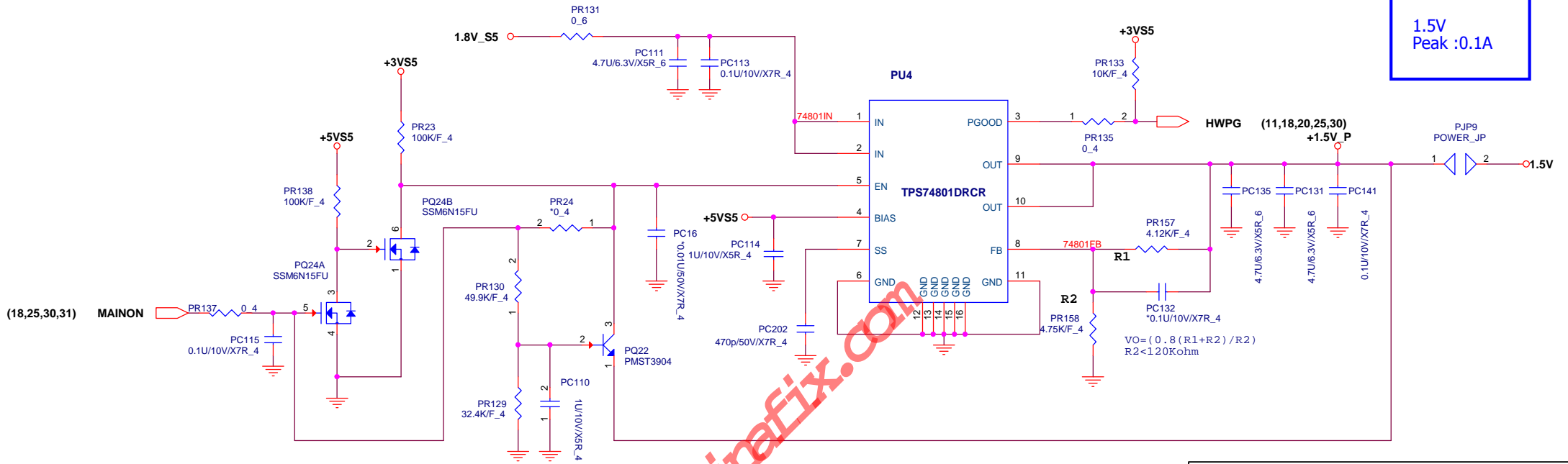


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Quanta Computer Inc.

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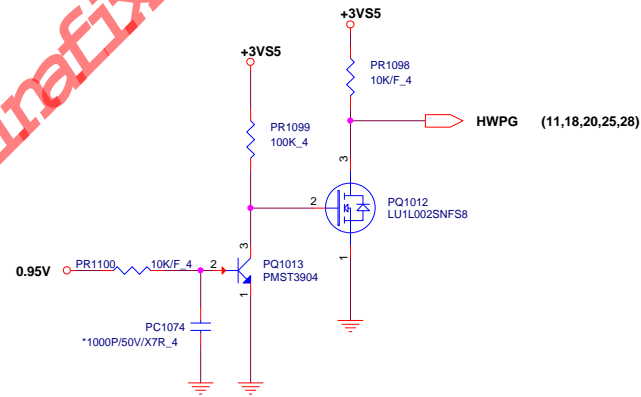
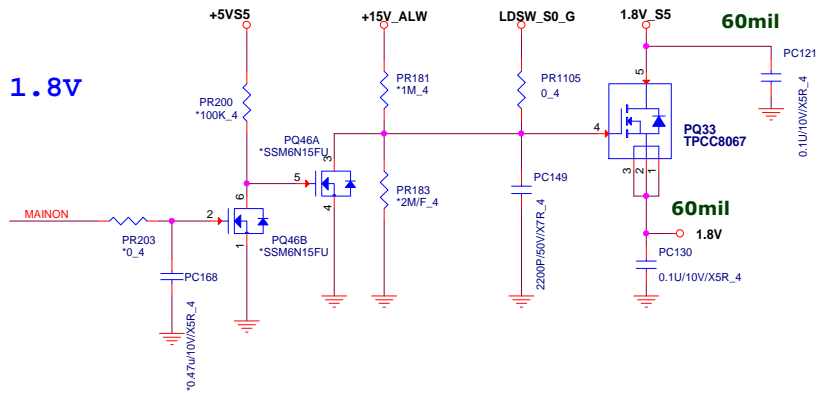
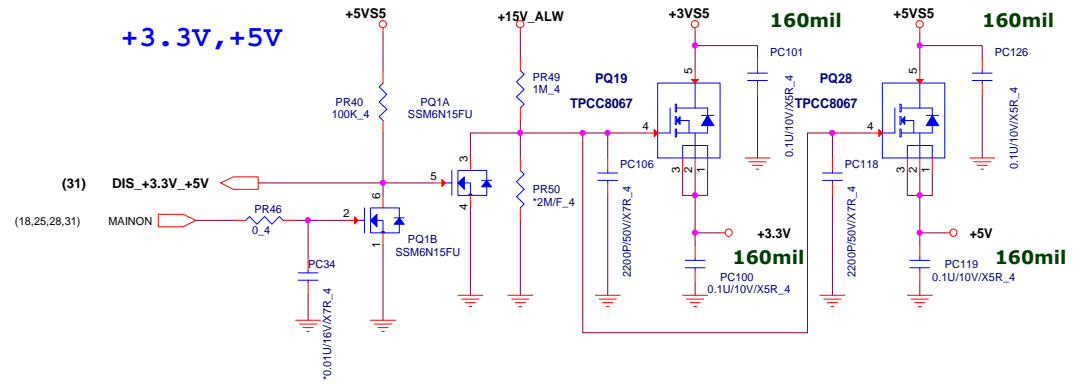
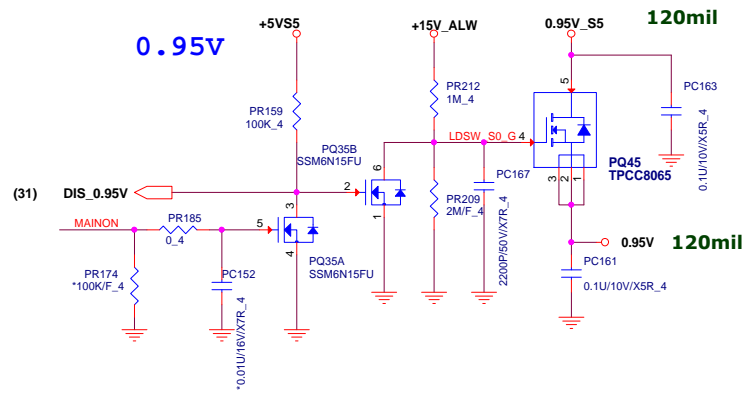
1.5V
Peak :0.1A



PROJECT : LIGJ
Quanta Computer Inc.

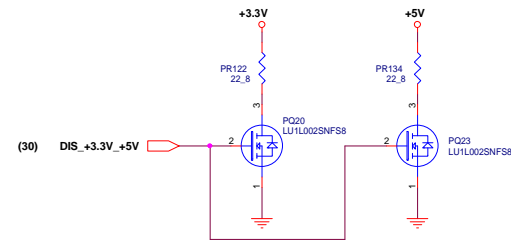
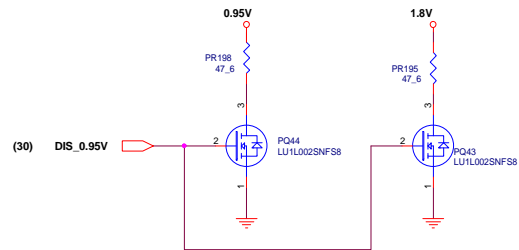
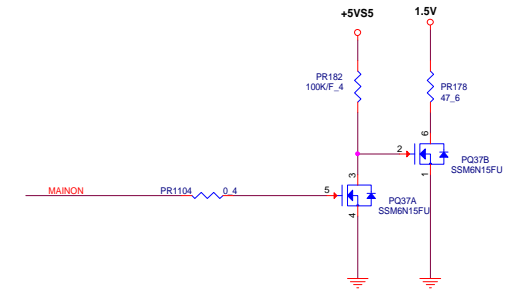
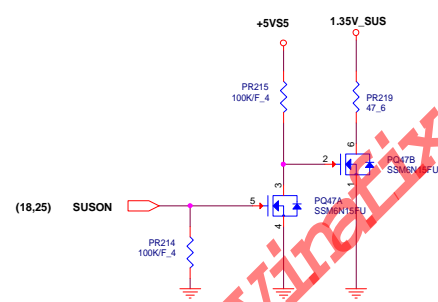
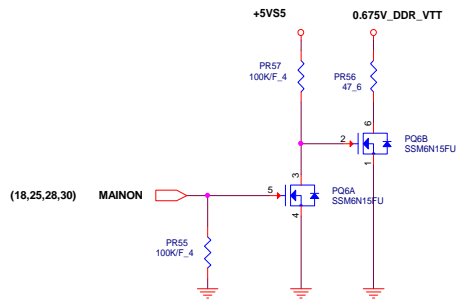
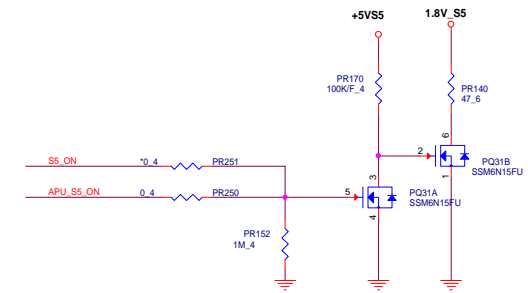
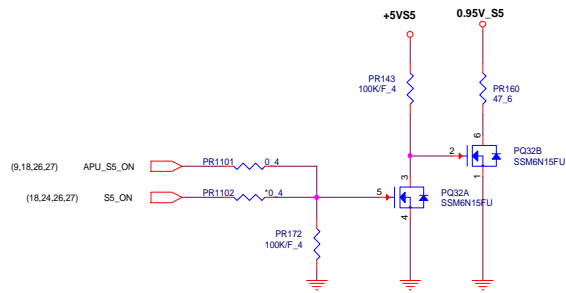
Size	Document Number	+1.5V (TPS74801)	Rev
	Custom		1A
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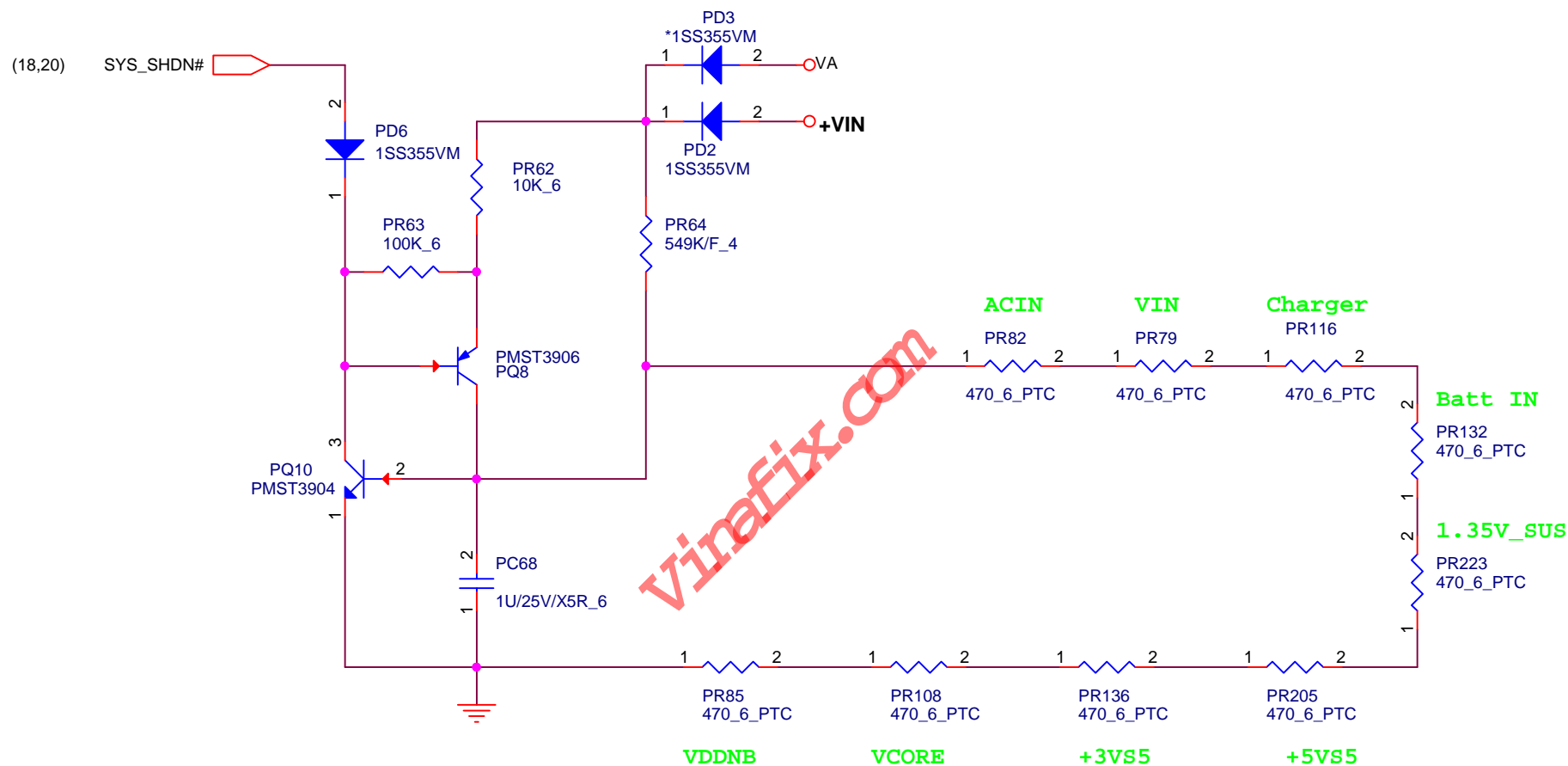
Load switch



PROJECT : LI6J
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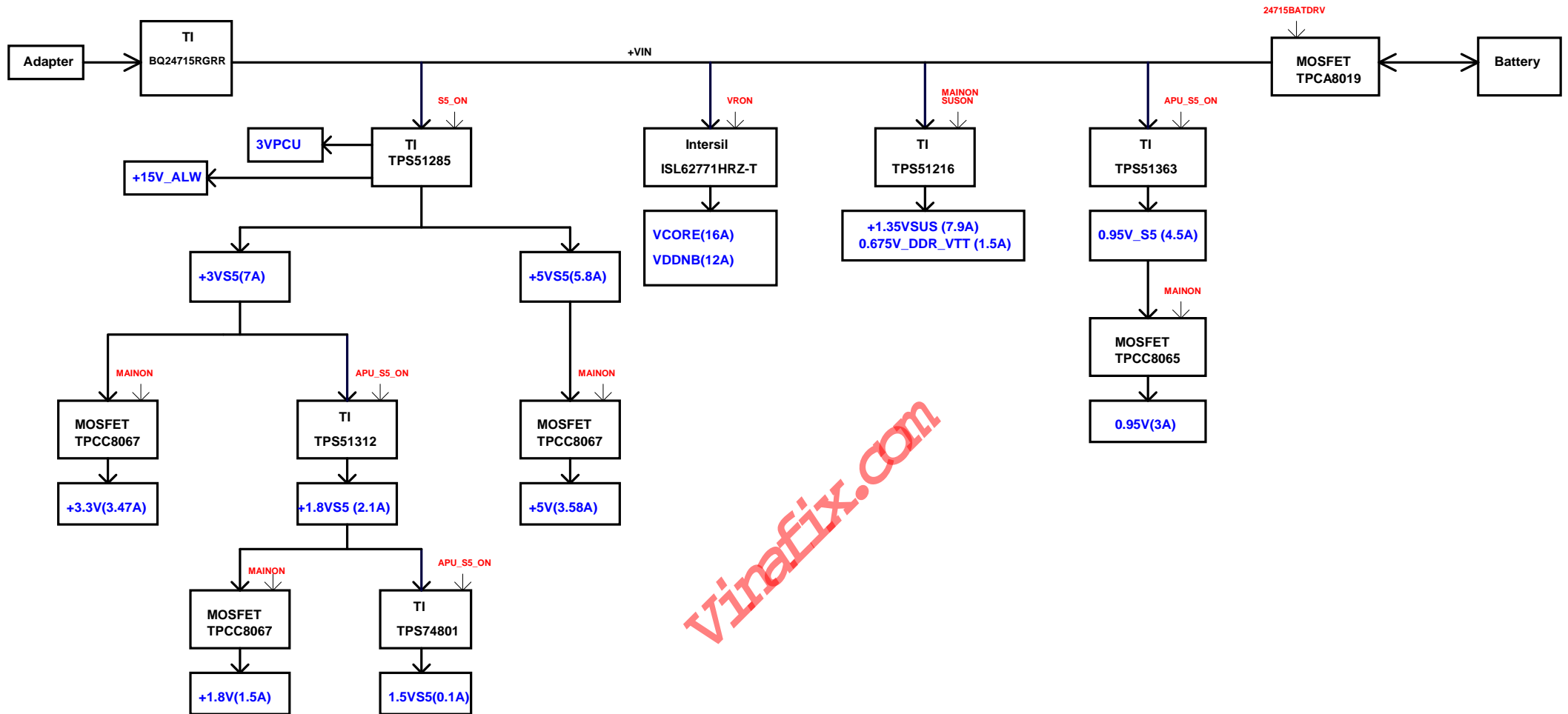
DISCHARGE

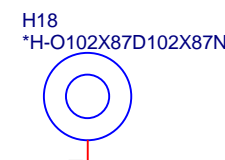
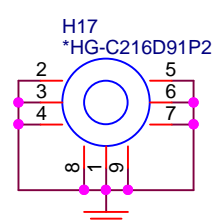
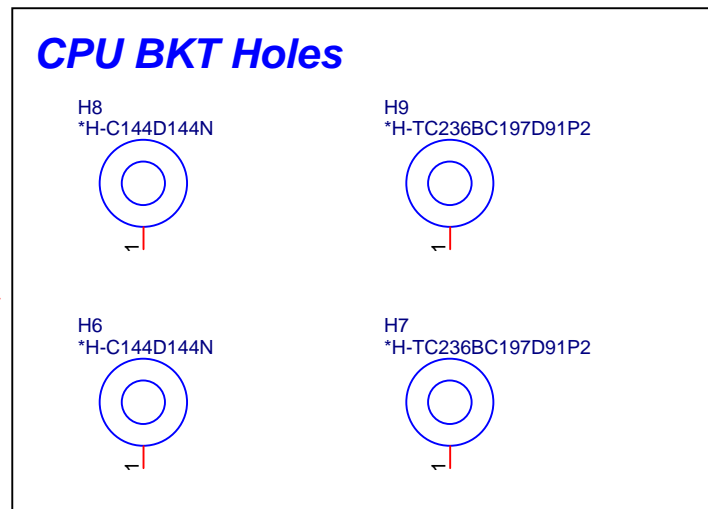
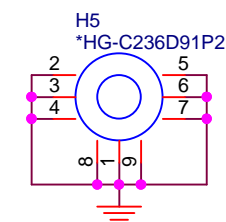
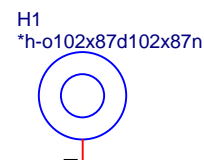
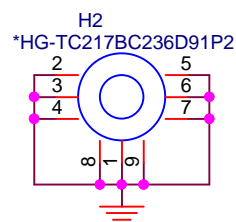
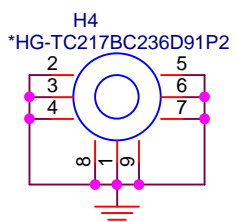
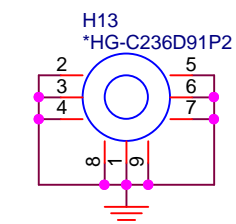
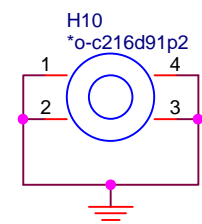
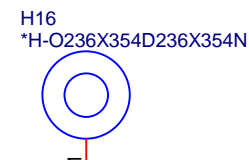
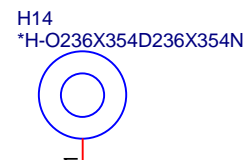
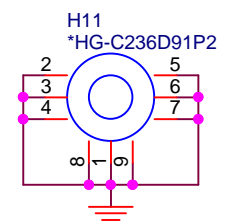
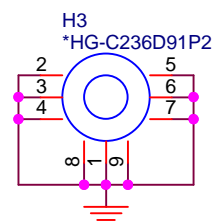




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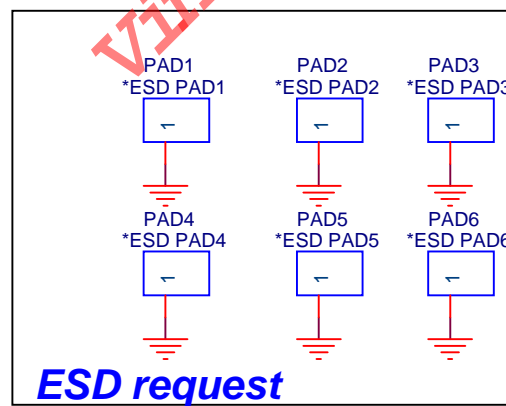
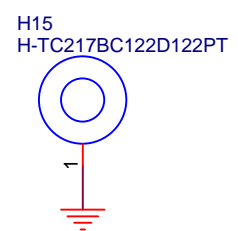
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Date: Thursday, August 07, 2014	Sheet 32	of 36



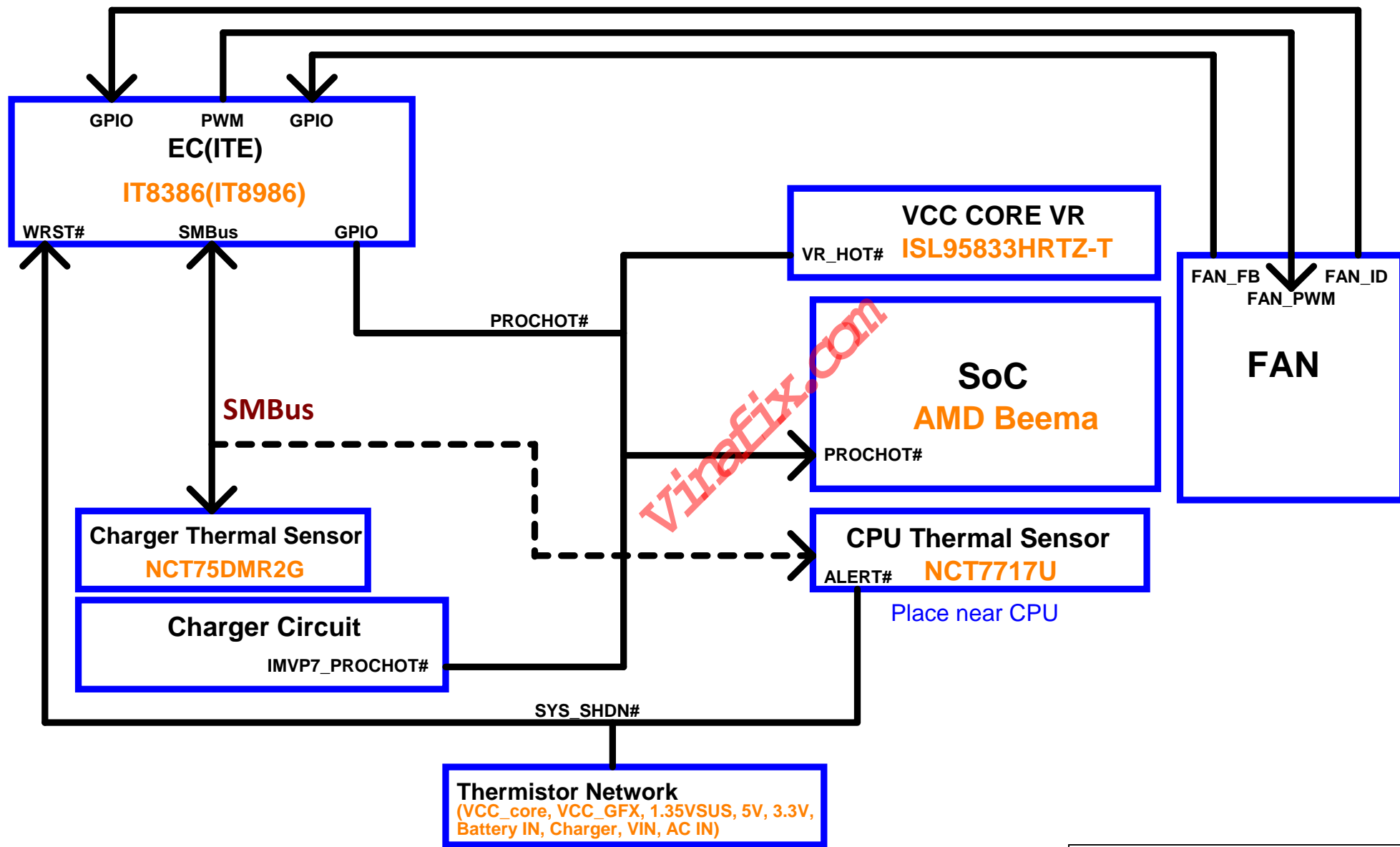


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